

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Paul Murtagh

Serial No.: To Be Assigned

Filed: Concurrently Herewith

For: DELAY-LOCKED LOOP (DLL) INTEGRATED CIRCUITS HAVING HIGH
BANDWIDTH AND RELIABLE LOCKING CHARACTERISTICS

Date: September 16, 2003

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

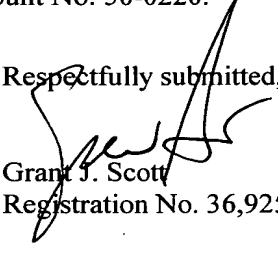
Sir:

Attached is a list of documents on Form PTO-1449, together with a copy of any listed foreign patent document and/or non-patent literature. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with the waiver by the U.S. Patent and Trademark Office of requirements under 37 C.F.R. § 1.98(a)(2)(i) for all U.S. national patent applications filed after June 30, 2003 and for all international applications that have entered the national stage under 35 USC § 371 after June 30, 2003.

It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.56 and Section 609 of the MPEP.

No fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

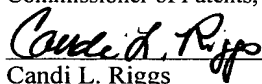

Grant J. Scott
Registration No. 36,925

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer No. 20792

CERTIFICATE OF MAILING UNDER 37 CFR § 1.10

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Candi L. Riggs

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)					Attorney Docket Number 5646-114		Serial No. To Be Assigned	
					Applicants: Paul Murtagh			
					Filing Date: Concurrently Herewith		Group	
U. S. PATENTS & PATENT APPLICATION PUBLICATIONS								
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate	
	1	6,593,786	7/15/03	Jung	327	158		
	2	6,586,978	7/1/03	Stief	327	158		
	3	6,584,578	6/24/03	Faue	713	503		
	4	6,584,021	6/24/03	Heyne et al.	365	194		
	5	6,539,072	3/25/03	Donnelly et al.	375	371		
	6	6,518,807	2/11/03	Cho	327	158		
	7	6,504,408	1/7/03	von Kaenel	327	158		
	8	6,501,328	12/31/02	Gauthier et al.	327	551		
	9	6,501,312	12/31/02	Nguyen	327	161		
	10	6,295,328	9/25/01	Kim et al.	375	376		
	11	2003/0154447	8/14/03	Gauthier et al.	716	2		
	12	2003/0154417	8/14/03	Drexler	713	400		
	13	2003/0151433	8/14/03	Takai	327	158		
	14	2003/0141910	7/31/03	Reindl	327	158		
	15	2003/0117194	6/26/03	Lee	327	158		
	16	2003/0117193	6/26/03	Lee	327	158		
	17	2003/0108139	6/12/03	Jung	375	376		
	18	2003/0099321	5/29/03	Juan et al.	375	376		
	19	2003/0095009	5/22/03	Gomm et al.	331	57		
	20	2003/0094984	5/22/03	Weis et al.	327	182		
	21	2003/0090296	5/15/03	Yoo	327	12		
	22	2003/0071668	4/17/03	Starr	327	157		
	23	2003/0067335	4/10/03	von Kaenel	327	158		
	24	2003/0058014	3/27/03	Krishnamurty	327	158		
	25	2003/0052719	3/20/03	Na	327	158		

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Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		Applicants: Paul Murtagh	
		Filing Date: Concurrently Herewith	Group
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)			
	26	Moon et al., "An All-Analog Multiphase Delay-Locked Loop Using a Replica Delay Line for Wide-Range Operation and Low-Jitter Performance," IEEE Journal of Solid-State Circuits, Vol. 35, No. 3, March 2000	

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